

DATASETS: ALGORITHM FOR VOLTAGE STABILITY CONTROL IN A POWER SYSTEM NETWORK WITH INTEGRATED MICROGRID

1. IEEE 9 BUS SINGLE LINE DIAGRAM IN RTDS

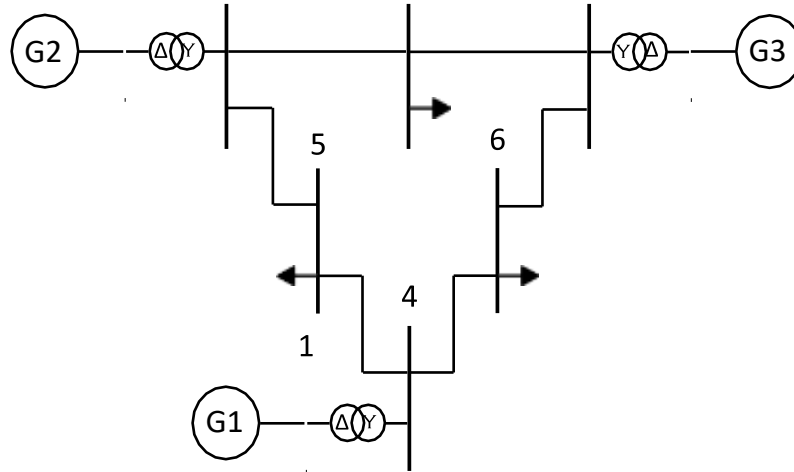


Figure 1: IEEE 9 bus system

2. RSCAD/RTDS SYSTEM DATA

Table 1: RSCAD Power Flow Data expressed in 100 MVA

BUS	Type	V (pu)	PG (MW)	QG (MVar)	PL (MW)	QL (MVar)
1	SLACK	1.040 $\angle 0.0^\circ$	71.6	27.0	-	-
2	P-V	1.025 $\angle 9.3^\circ$	163.0	6.7	-	-
3	P-V	1.025 $\angle 4.7^\circ$	85.0	-10.9	-	-
4	P-Q	1.026 $\angle -2.2^\circ$	-	-	-	-
5	P-Q	0.996 $\angle -4.0^\circ$	-	-	125.0	50.0
6	P-Q	1.013 $\angle -3.7^\circ$	-	-	90.0	30.0
7	P-Q	1.026 $\angle 3.7^\circ$	-	-	-	-
8	P-Q	1.016 $\angle 0.7^\circ$	-	-	100.0	35.0
9	P-Q	1.032 $\angle 2.0^\circ$	-	-	-	-

Table 2: IEEE 9 bus Line data in RSCAD

From BUS	To BUS	R (pu)	X (pu)	B (pu)
4	5	0.0100	0.0850	0.1760
4	6	0.0170	0.0920	0.1580
5	7	0.0320	0.1610	0.3060
6	9	0.0390	0.1700	0.3580
7	8	0.0085	0.0720	0.1490
8	9	0.0119	0.1008	0.2090

Table 3: Transformer Data

From BUS	To BUS	R (pu)	X (pu)	Tap Ratio ¹
1	4	0.0	0.0576	1.0
2	7	0.0	0.0625	1.0
3	9	0.0	0.0586	1.0

Table 4: Generator Data-1 (100 MVA Base)

GEN	BUS	Xa (pu)	Xd (pu)	Xd' (pu)	Xd'' (pu)	Xq (pu)	Xq' (pu)	Xq'' (pu)
1	5	0.01460	0.1460	0.0608	0.06	0.1000	0.0969	0.06
2	7	0.08958	0.8958	0.1198	0.11	0.8645	0.1969	0.11
3	9	0.13125	1.3125	0.1813	0.18	1.2578	0.2500	0.18

Table 5: Generator Data-2 (100 MVA Base)

GEN	BUS	Ra (pu) ²	Tdo' (s)	Tdo'' (s)	Tqo' (s)	Tqo'' (s)	H (s)	D(pu/pu)
1	5	0.000125	8.96	0.01	0.310	0.01	23.64	0.0
2	7	0.000125	6.00	0.01	0.535	0.01	6.40	0.0
3	9	0.000125	5.89	0.01	0.600	0.01	3.01	0.0

Table 6: Exciter Data-1 (IEEE Type DC1A)

GEN	KA	TA	VRmin	Vrmax	KE	TE	KF	TF
1	20.0	0.2	-5.0	5.0	1.0	0.314	0.063	0.35
2	20.0	0.2	-5.0	5.0	1.0	0.314	0.063	0.35
3	20.0	0.2	-5.0	5.0	1.0	0.314	0.063	0.35

Table 7: Exciter Data-2 (IEEE Type DC1A)

GEN	EX1	S(EX1)	EX2	S(EX2)
2	3.3	0.6602	4.5	4.2662
3	3.3	0.6602	4.5	4.2662
4	3.3	0.6602	4.5	4.2662

Table 8: Governor Data (TGOV1)

GEN	R	T1	Vmax	Vmin	T2	T3	Dt
1	0.05	0.05	5.00	-5.00	2.1	7.0	0.0
2	0.05	0.05	5.00	-5.00	2.1	7.0	0.0
3	0.05	0.05	5.00	-5.00	2.1	7.0	0.0

Table 9: Power consumption per load in RSCAD

Load	Bus	P [MW]	Q [Mvar]
Load A	Bus 5	125	50
Load B	Bus 6	90	30
Load C	Bus 8	100	35

3. PHOTOVOLTAIC CONTROL DESIGN IN RTDS

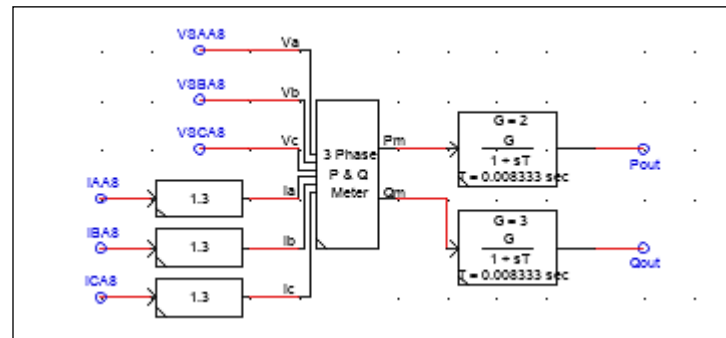


Figure 1: Power measurement at VSC

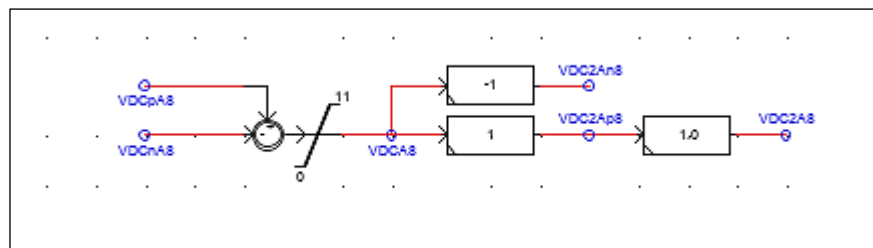


Figure 2: Logic to control the limit of PV voltage

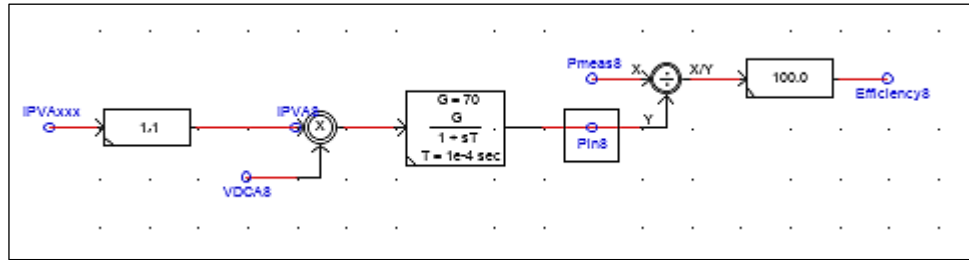


Figure 3: PV efficiency measurement logic

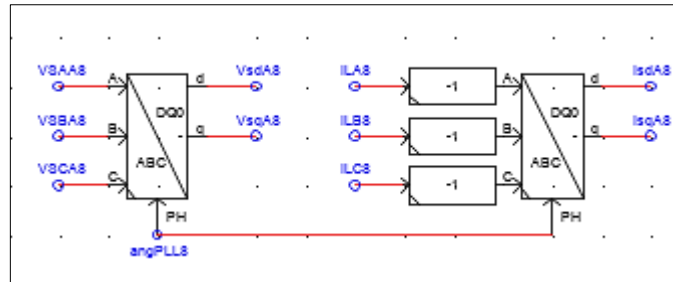


Figure 4: ABC to dq frame terminal logic

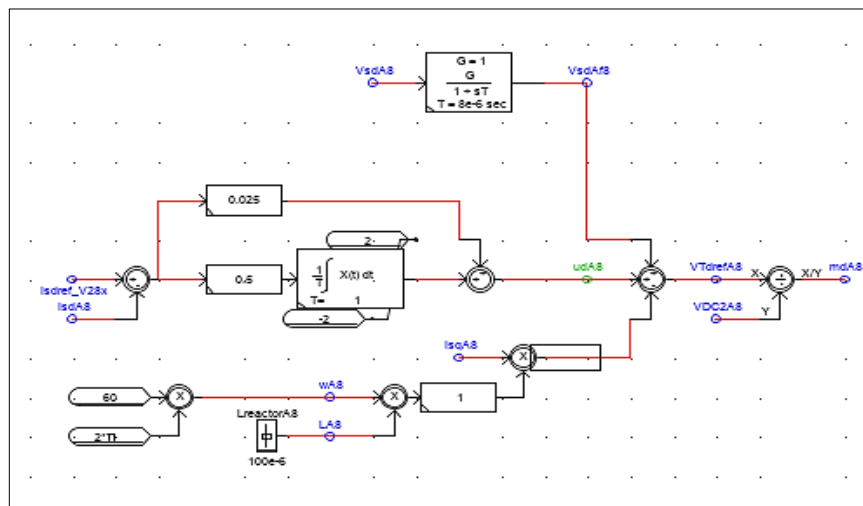


Figure 5: Inner loop dq current control

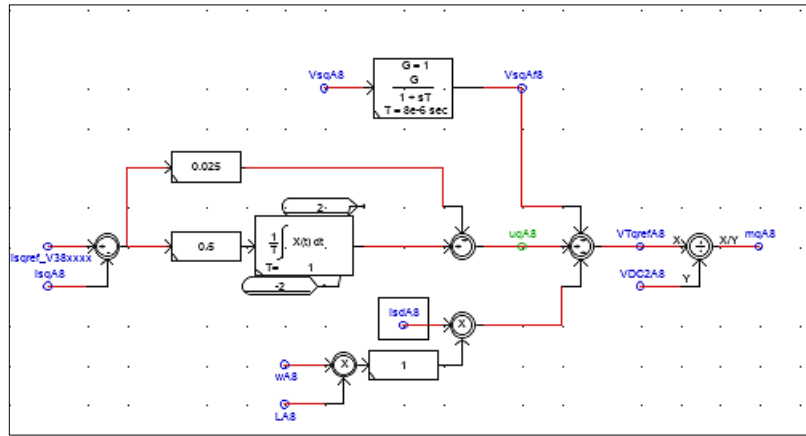


Figure 6: Inner loop dq current control

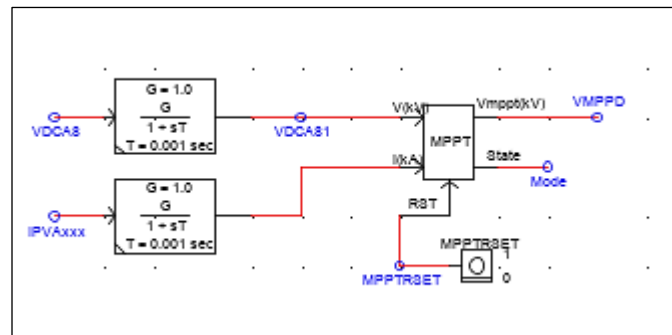


Figure 7: MPPT outer loop control

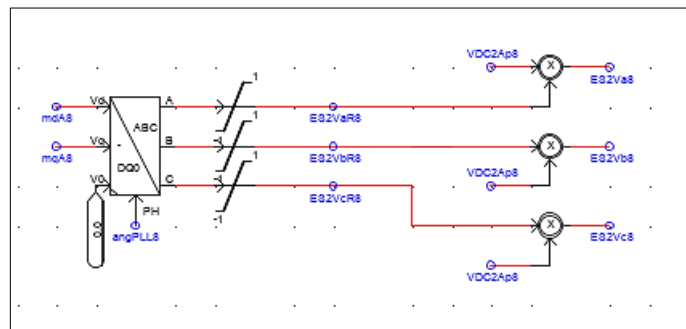


Figure 8: A reference wave generator

4 VOLATGES PROFILES

4.1 voltage Profiles under disturbances.

Table 4 1: Real-time results under disturbance compared to results under normal conditions.

Modified 9 bus system base case simulation results in RSCAD/RTDS			Modified 9 bus system results after disturbance in RSCAD/RTDS	
Bus	u, Magnitude [p.u.]	TYPE	Bus	u, Magnitude [p.u.]
1	1.030	SLACK	1	1.025
2	0.9946	P-V	2	0.9704
3	1.018	P-V	3	0.9878
4	1.012	P-Q	4	0.9872
5	0.9777	P-Q	5	0.9199
6	0.9984	P-Q	6	0.9463
7	1.001	P-Q	7	0.9598
8	0.9957	P-Q	8	0.9442
9	1.020	P-Q	9	0.9744

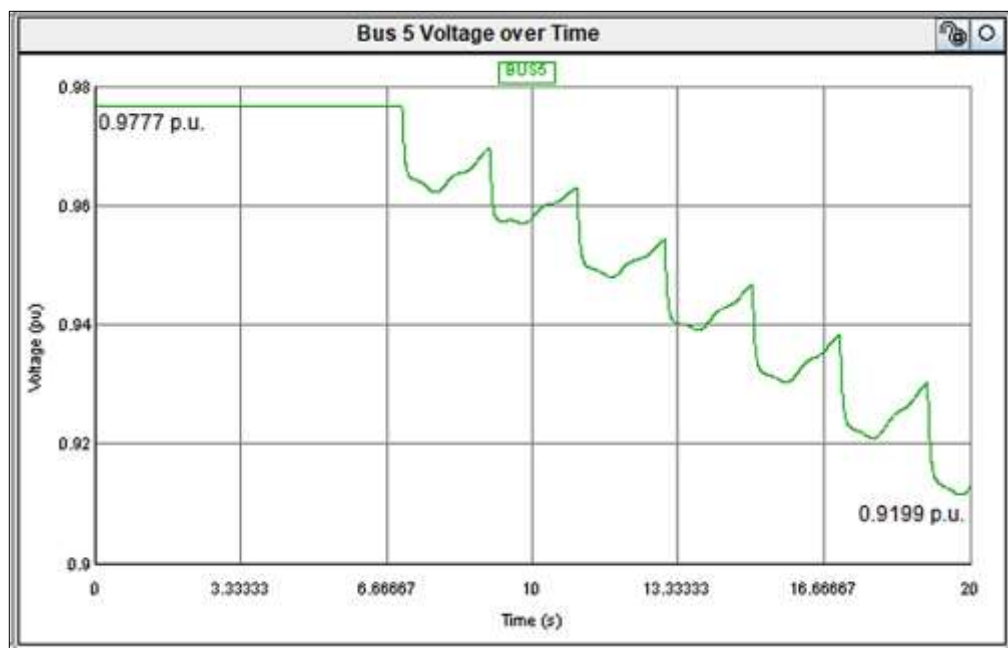


Figure 4 1: Voltage drop at bus 6 due to disturbance caused by 35% increase of load demand

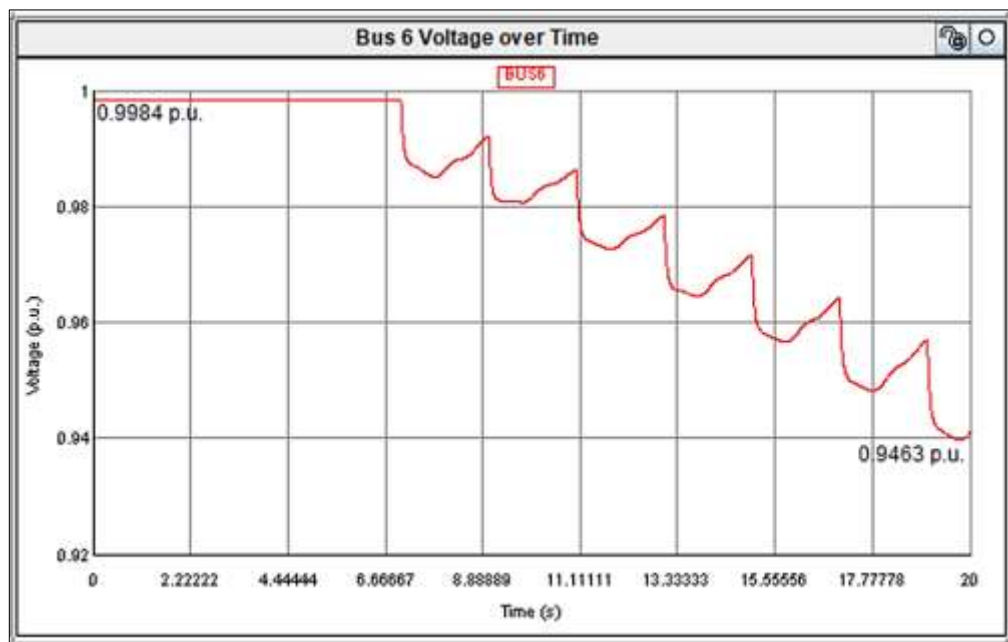


Figure 4 2: Voltage drop at bus 6 due to disturbance caused by 35% increase in load demand

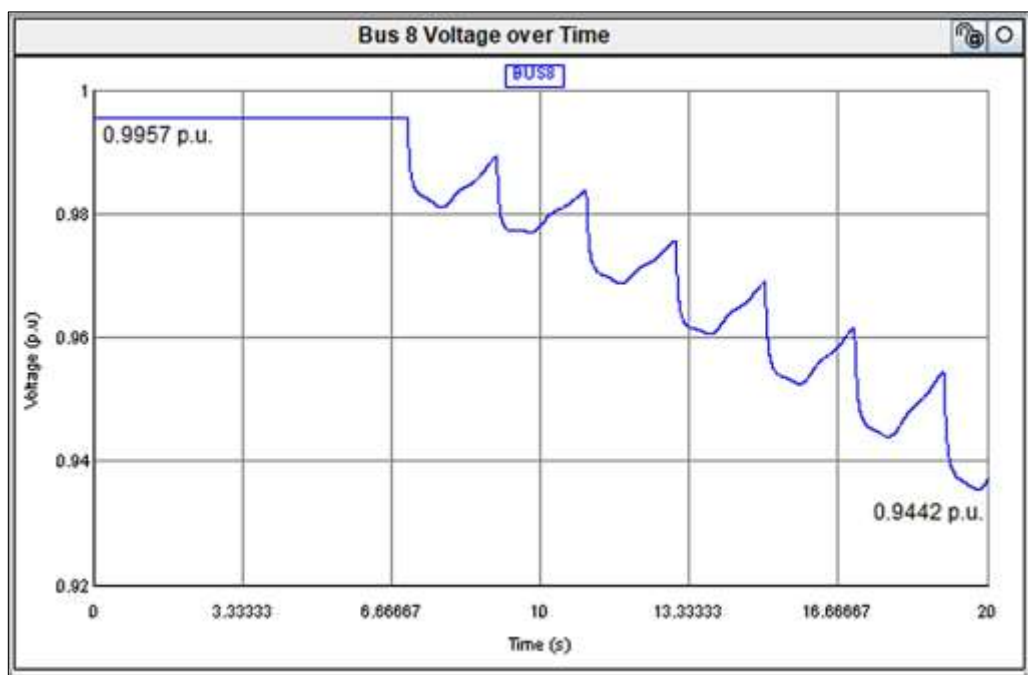


Figure 4 3: Voltage drops at bus 6 due to disturbance caused by a 35% increase in load demand

4.2 Voltages profiles after PV integration

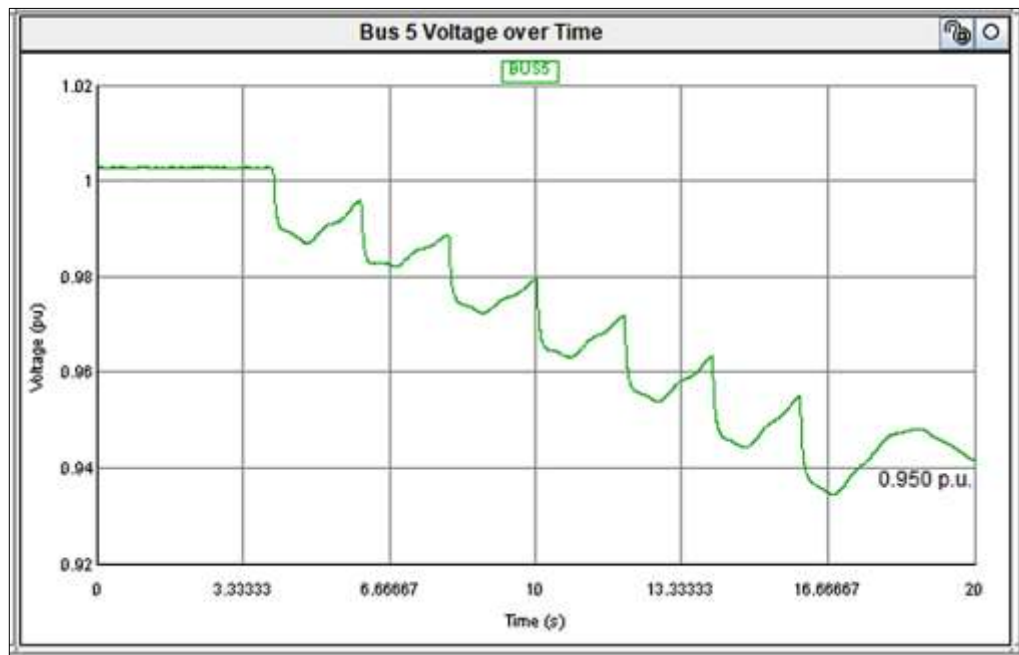


Figure 4.4: Voltage recovering at bus 5 when PV action is simulated for 20 second

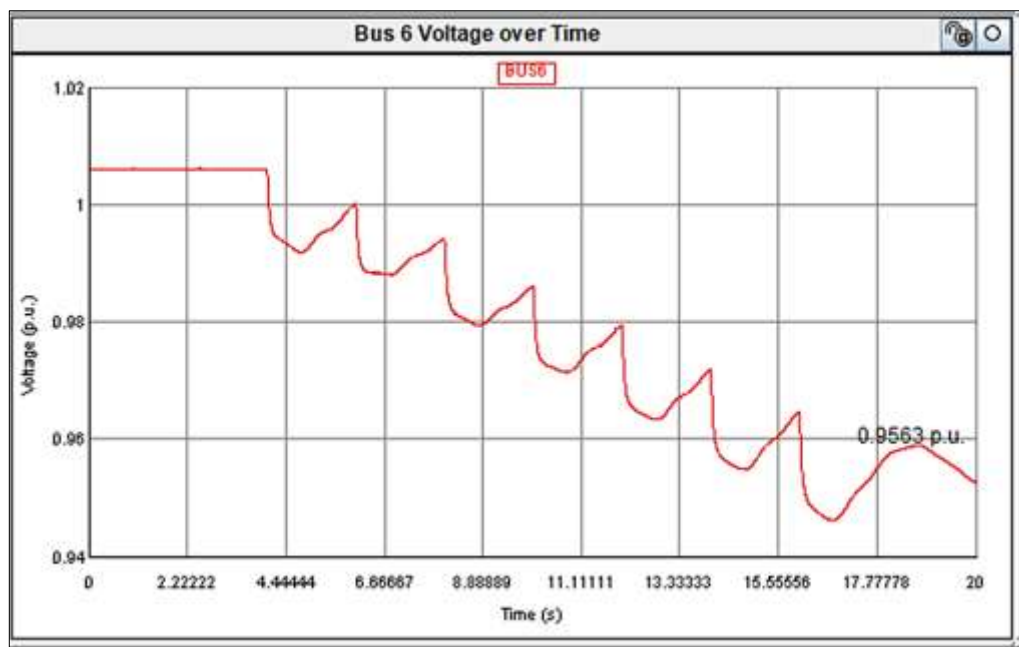


Figure 4.5: Voltage recovering at bus 6 when PV action is simulated for 20 second

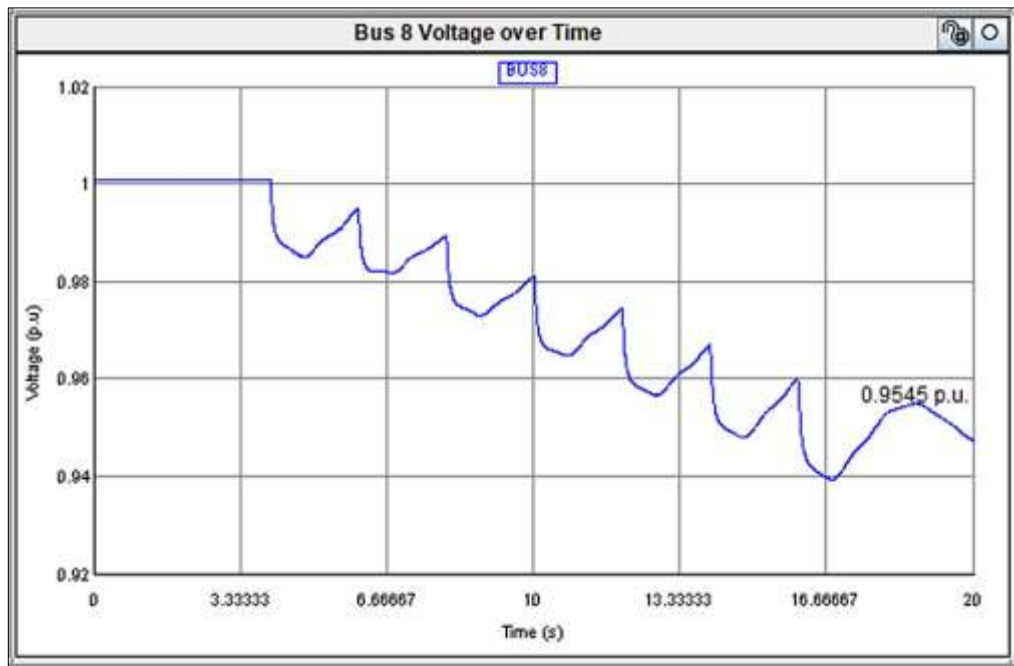


Figure 4.6: Voltage recovering at bus 8 when PV action is simulated for 20 second

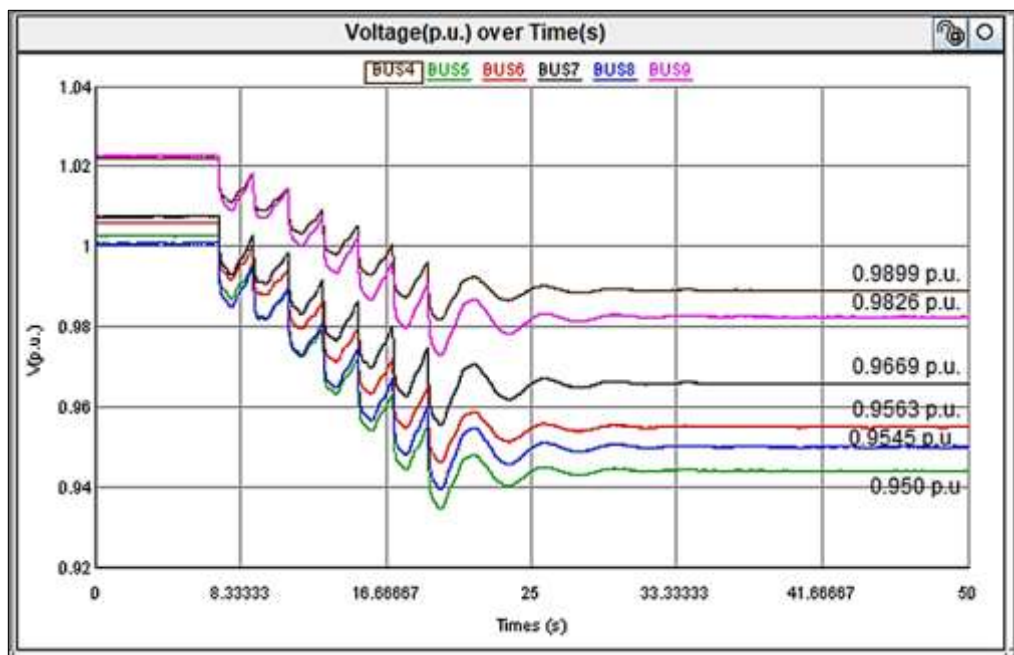


Figure 4.7: Voltage recovery of all buses due to PV penetration